What is claimed is:

1. A method for compensating non-linearity errors in A/D converter conversion operations associated with converting analog image data from a CMOS imager to digital data, comprising:

(a) isolating an A/D converter from the CMOS imager;

(b) applying a plurality of analog voltages to the isolated A/D converter, the plurality of voltages ranging from analog ground to a full-scale voltage level;

(c) measuring and storing a difference between an output from the isolated A/D converter and a reference value associated with the analog voltage being applied to the isolated A/D converter; and

(d) correcting the non-linearity of the isolated the isolated A/D converter using the stored difference.

2. The method as claimed in claim 1, wherein the plurality of applied analog voltages are analog ground, 0.25 of the full-scale voltage level, 0.5 of the full-scale voltage level, 0.75 of the full-scale voltage level, and the full-scale voltage level.

3. A circuit for compensating errors in correlated double sampling amplifiers and/or A/D converters associated with a CMOS imager having columns of pixels, comprising:

a reference voltage source to produce test voltages;

a test switch operatively connected between said reference voltage source and a correlated double sampling amplifier;

a test switch control line, operatively connected to said test switch, to apply a signal to said test switch, said signal controlling an ON/OFF state of said test switch, said test switch applying a test voltage from said reference voltage source to the correlated double sampling amplifier when the state of said test switch is ON; and

a measurement circuit to measure a difference between an output of the A/D converter produced from a test voltage being applied to the correlated double sampling amplifier through said test switch and a reference voltage associated with the applied test voltage to determine an error in the correlated double sampling amplifier and/or A/D converter.

4. The circuit as claimed in claim 3, further comprising:

an isolation switch operatively connected between a column of pixels and an associated correlated double sampling amplifier to effectively electrically isolate the column of pixels from the associated correlated double sampling amplifier;

said isolation switch being in an OFF state when said test switch is in an ON state.

5. The circuit as claimed in claim 3, wherein said reference voltage source produces a voltage corresponding to a full-scale voltage level to enable said measurement circuit to determine a gain error in the correlated double sampling amplifier and/or A/D converter.

6. The circuit as claimed in claim 3, wherein said reference voltage source produces a voltage corresponding to ground to enable said measurement circuit to

determine an offset error in the correlated double sampling amplifier and/or A/D converter.

7. The circuit as claimed in claim 3, wherein said reference voltage source produces a sequence of two voltages with a difference corresponding to a full-scale voltage level minus a predetermined maximum anticipated variation voltage to enable said measurement circuit to determine a gain error in the correlated double sampling amplifier and/or A/D converter.

8. The circuit as claimed in claim 7, wherein said predetermined maximum anticipated variation voltage corresponds to maximum gain variations.

9. The circuit as claimed in claim 3, wherein said reference voltage source produces a sequence of two voltages with a difference corresponding to a predetermined voltage to enable said measurement circuit to determine an offset error in the correlated double sampling amplifier and/or A/D converter.

10. The circuit as claimed in claim 9, wherein said predetermined voltage corresponds to maximum offset variations.

11. The circuit as claimed in claim 3, wherein said reference voltage source produces a plurality of analog voltages ranging from analog ground to a full-scale voltage level to enable said measurement circuit to determine non-linearity errors in the A/D converter.

12. The circuit as claimed in claim 3, wherein said reference voltage source produces a voltage corresponding to a full-scale voltage level to enable said measurement circuit to determine a gain error in the correlated double sampling amplifier and/or A/D converter;

said reference voltage source producing a voltage corresponding to ground to enable said measurement circuit to determine an offset error in the correlated double sampling amplifier and/or A/D converter; and

said reference voltage source producing a plurality of analog voltages ranging from analog ground to a full-scale voltage level to enable said measurement circuit to determine non-linearity errors in the A/D converter.